CLAIMS:

1. A method of operating a data processing device (100), notably a chip card, which includes an integrated circuit (10) which carries out, in dependence on a clock signal, arithmetic operations, notably cryptographic operations, data input and data output (38) as well as data transfer (40) from and to registers of the integrated circuit (10), characterized in that
the integrated circuit (10) is controlled in such a manner that the execution of arithmetic operations on the one hand and the data input/output (38) as well as the data transfer (40) from one register to another or between registers (30, 32) on the other hand is executed in parallel in time.

2. A method as claimed in Claim 1,
characterized in that
directly before, during and/or directly after the data transfer from one register to another or between the registers (30, 32) of the integrated circuit, a processor (28) of the integrated circuit (10) executes dummy calculations which act on random or predetermined data, no data being written into registers (30, 32) of the integrated circuit.

3. A data processing device (100), notably a chip card, which is specifically intended to carry out a method as claimed in at least one of the preceding Claims, and includes an integrated circuit (10) which executes arithmetic operations, notably cryptographic operations, in dependence on a clock signal (20), the integrated circuit (10) including a processor (28) with an associated first register (30) and data inputs and outputs (24, 26),
characterized in that
a second register (32) is connected to the first register (30) and is provided with the data inputs and outputs (24, 26), a control unit (16) being connected to the integrated circuit (10) and being constructed in such a manner that it controls parallel operation in time of the registers (30, 32) for data input/output (38) and data transfer (40) from register to register or

between the registers (30, 32) on the one hand and arithmetic operations (40) of the processor (28) on the other hand.

4. A data processing device (100) as claimed in Claim 3, characterized in that the first register (30) is an operand register of the processor (28) and/or the second register (32) is an operand register for the data input/output (38).

LIST OF REFERENCES

100	data processing device
10	integrated circuit
12	register
14	program access
16	control unit
18	lead
20	clock signal
22	control leads
24	data inputs
26	data outputs
28	processor
30	first operand register R1
32	second operand register R2
34	time base
36	calculation
38	data input and data output
40	data transfer R1-2
42	data transfer R2-1